CLAIMS

1. A laminated flip-chip interconnect package comprising a substrate having a chip attach surface and a board attach surface that define contact pads for attachment to corresponding pads on the chip and board, wherein the substrate board attach surface comprises at least one solid plane covering the chip attach surface region near at least one chip corner, said solid plane comprising a dielectric material.

2. A laminated flip-chip interconnect package according to claim 1 wherein said dielectric material is covered with a layer of material selected from a soldermask and a coverlay material.

3. A laminated flip-chip interconnect package according to claim 2 wherein said layer of material is selected from the group consisting of polyimide, polytetrafluoroethylene, and expanded polytetrafluorethylene impregnated with cyanate ester and epoxy.

4. A laminated flip-chip interconnect package comprising a substrate having a chip attach surface and a board attach surface that define contact pads for attachment to corresponding pads on the chip and board, wherein the substrate board surface comprises at least one solid plane covering the chip attach surface region near the chip corners, said solid plane comprising a metal.

5. A laminated flip-chip interconnect package according to claim 4 wherein said metal is selected from the group consisting of copper, silver, gold and aluminum.

6. A laminated flip-chip interconnect package according to claim 4 wherein said metal is covered with a layer of material selected from a soldermask and a coverlay material.

7. A laminated flip-chip interconnect package according to claim 6 wherein said layer of material is selected from the group consisting of polyimide, polytetrafluoroethylene, and expanded polytetrafluorethylene impregnated with cyanate ester and epoxy.

8. A laminate flip-chip interconnect package according to claim 4 wherein said soldermask has a plurality of openings defining ball grid array pads.